and with the sum (e.g., 60 GHz) being filtered. Outputs from the demodulator 310 are supplied via an amplifier 324 and a microstrip line to coaxial connector 326 to produce an intermediate frequency output 328 constituting a demodulated, received signal. As with Figure 1, noise figures and gain figures at each point along the transmission paths shown are illustrated. The intermediate frequency output 328 can be transmitted to a modem.

A single receiver voltage regulator can be used in connection with the Figure 3 receiver. A DC voltage regulator for the receiver is illustrated in Figure 4.

Referring to Figure 4, a receiver voltage regulator 400 includes a voltage input 402, on the order of 5.5 volts or greater. This input is supplied via a voltage stabilizing and filter network which includes diode 404, resistor 406, Zener diode 408, capacitor 410 and capacitor 412, to an input 414 of a positive voltage regulator 416. The positive voltage regulator 416 includes a shutdown input 418, an adjustment input 420 and an output 422. A feedback resistor 424 is connected between the input 414 and the shutdown 418. The adjustment input 420 is controlled by a voltage divider that includes a resistor 426 and an adjustable resistor 428. The output of the positive voltage regulator is supplied to a DC drain bias output on the order of 4 volts via filter capacitors 430 and 432.

The shutdown input 418 is controlled by a MOSFET, such as a transistor 436 designated 2N4393 available from Solitron Corp., whose drain is grounded and whose collector is connected to the shutdown input. A gate of the transistor 436 is connected via a resistor 438 to the output of a negative voltage regulator 440 configured similar to that of the negative voltage regulator in Figure 2 The output of the negative voltage regulator 440, designated V_y at node 442, is supplied via a resistor 444 to a gate bias output 446, on the order of -3 volts. The negative voltage regulator 440 is driven at its input by an input voltage on the order of -6 volts or less, supplied via a voltage stabilizing and filter network which includes a reverse biased diode 448, a resistor 450, and a parallel combination of a Zener diode 452, a capacitor 454 and a capacitor 456. The negative voltage regulator 440 can be adjusted via a voltage divider that includes a resistor 458 and an adjustable resistor 460. The output of the negative voltage

regulator is supplied to the gate bias output 446 via a filter network which includes capacitors 462, 464, and a voltage divider network that includes resistor 444 and resistor 466.

As with the Figure 2 transmitter regulator, the Figure 4 receiver regulator only provides the drain bias output when an appropriate voltage V_y is present at the node 442, and an appropriate gate bias is present at output 446. Operation of the Figure 4 regulator with respect to a shutdown of the positive voltage regulator 416, is similar to the operation described with respect to the Figure 2 regulator.

Figures 5A and 5B show an exemplary frequency plan for establishing the RF input 110 of the Figure 1 transmitter. As shown in Figure 5A, the frequency plan 500 exploits a dual polarization feature used in accordance with the exemplary embodiments of the present invention. More particularly, exemplary embodiments use a dual polarization antenna design to provide transmitter isolation with respect to the receiver and vice versa. Exemplary embodiments can use a single antenna with an isolator, or can use two separate antennae separated by a distance.

In the Figure 5A frequency plan, the transmitter input frequencies include a Group A intermediate frequency on the order of 2.35 GHz, and a Group B intermediate frequency of 3.205 GHz. The receiver intermediate frequencies output therefrom include a Group A frequency of 3.025 GHz, and a Group B frequency of 2.325 GHz, with a 700 MHz separation, as shown in Figure 5B. As such, information can be transmitted over a forward channel using a first operating frequency, while at the same time, information can be received by the transceiver via a second intermediate frequency associated with a reverse channel.

In the Figure 5A frequency plan, transmitted Group A frequencies are modulated in a modulator 502 via the local oscillator signal, and are demodulated via a demodulator 504 using, for example, the same local oscillator. Signals are transmitted and received via respective amplifiers and filters.

The Group B frequencies are received via a demodulator 506, and are transmitted with a modulator 508. In accordance with exemplary embodiments of the present invention, both the demodulator and modulator are driven by the same local

oscillator although separate local oscillators can, of course, be used. Signals are transmitted and received via the use of filters and amplifiers in the respective transmission and reception paths. As a result, forward and reverse channels 510 and 512, respectively, are established.

The local oscillator can be configured to satisfy the transmitter and receiver specifications set forth herein in any known fashion. In accordance with exemplary embodiments described herein, the exciter receives a reference input frequency of, for example, 50 MHz and a reference input power of 10 dB minimum. The reference input power is provided via a phase locked oscillator coherent with the system reference oscillator. A synthesized output frequency of the exciter is, for example, on the order of 1.2 to 2.525 GHz using 14 channels with 25 MHz spacing, or any other desired frequency and/or spacing.

The local oscillator output can be frequency divided into two channels to provide two outputs, each designated LO/2, having a frequency on the order of 18 GHz (e.g., 18.15 to 18.475 GHz), using 14 channels with 25 MHz spacing. The output power level for the LO/2 output is on the order of 10 to 16 dB, and can be buffered by a saturated amplifier. Exemplary single sideband phase noise for each LO/2 output can, for example, be as follows: -88 dBc/Hz at 100 Hz, -98 dBc/Hz at 100 kHz, -103 dBc/Hz at 10 kHz, -105 dBc/Hz at 100 kHz, and -108 dBc/Hz at 1 MHz. Exciter output port-to-port isolation can be, for example, 20 dB or any other specified isolation. Exciter spurious and harmonic outputs can be on the order of -70 dBc. The exciter output frequency tolerance can be on the order of $\pm$ 0.6 parts per minute (ppm), and the frequency switching time can be on the order of 1 millisecond. Of course, these values can be varied as desired.

Although any conventional exciter design can be used, Figure 6 illustrates one exemplary embodiment. The Figure 6 exciter 600 includes a 50 MHz input from a frequency reference oscillator 602. This reference oscillator frequency is supplied to a phase lock loop chip (PLL chip 604) where it is frequency divided by four via a divider 606, and supplied to a multiplexer 608. The multiplexer 608 receives a feedback signal via an N (e.g., N=4) divider 610. Outputs from the multiplexer 608 are supplied to an